Search History

STN
(HCAPLUS, INSPEC, USPATFULL)
2/1/05

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PI US 2004123796 A1 20040701
AI US 2003-467566 A1 20031009 (10)
WO 2002-JP1159 20020212
PRAI JP 2001-36604 20010214
JP 2001-98870 20010330
JP 2001-274376 20010911
DT Utility
FS APPLICATION
LREP MCGINN & GIBB, PLLC, 8321 OLD COURTHOUSE ROAD, SUITE 200, VIENNA, VA, 22182-3817
CLMN Number of Claims: 55
ECL Exemplary Claim: 1
DRWN 11 Drawing Page(s)
LN.CNT 2270
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L8 ANSWER 2 OF 2 USPATFULL on STN
AB A **seed layer** as a **laminate** of a GaN **layer** (second **seed layer**) and an AlN buffer **layer** (first **seed layer**) is formed on a sapphire substrate. A front surface thereof is etched in the form of stripes with a stripe width (seed width) of about 5 μm, a wing width of about 15 μm and a depth of about 0.5 μm. As a result, mesa portions each shaped like nearly a rectangle in sectional view are formed. Non-etched portions each having the seed multilayer as its flat top portion are arranged at arrangement intervals of L≈20 μm. Part of the sapphire substrate is exposed in trough portions of wings. The ratio S/W of the seed width to the wing width is preferably selected to be in a range of from about 1/3 to about 1/5. Then, a **semiconductor** crystal A is grown to obtain a thickness of not smaller than 50 μm. The **semiconductor** crystal is separated from the **starting substrate** to thereby obtain a high-quality single crystal independent of the **starting substrate**. When a **halide vapor phase** epitaxy method is used in the condition that the V/III ratio is selected to be in a range of from 30 to 80, both inclusively, a **semiconductor** crystal free from cracks can be obtained.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:22568 USPATFULL
TI Method for producing **semiconductor** crystal
IN Nagai, Seiji, Nishikasugai-gun, JAPAN
Kojima, Akira, Nishikasugai-gun, JAPAN
Tomita, Kazuyoshi, Nagoya-shi, JAPAN
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PI US 2004016396 A1 20040129
AI US 2003-620970 A1 20030717 (10)
PRAI JP 2002-210806 20020719
DT Utility
FS APPLICATION
LREP McGinn & Gibb, PLLC, Suite 200, 8321 Old Courthouse Road, Vienna, VA, 22182-3817
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 1 Drawing Page(s)
LN.CNT 679
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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=> d 18 1-2 abs,bib

L8 ANSWER 1 OF 2 USPATFULL on STN

AB When a substrate layer (desired **semiconductor** crystal) made of a **group III nitride** compound is grown on a base substrate comprising a lot of projection parts, a cavity in which a **semiconductor** crystal is not deposited may be formed between each projection part although it depends on conditions such as the size of each projection part, arranging interval between each projection part and crystal growth. So when the thickness of the substrate layer is sufficiently larger compared with the height of the projection part, inner stress or outer stress become easier to act intensively to the projection part. As a result, such stress especially functions as shearing stress toward the projection part. When the shearing stress becomes larger, the projection part is ruptured. So utilizing the shearing stress enables to separate the base substrate and the substrate layer easily. The larger the cavities are formed, the more stress tends to concentrate to the projection parts, to thereby enable to separate the base substrate and the substrate layer more securely.

A reaction prevention layer is formed to prevent Si from reacting with a gallium nitride group **semiconductor**. By forming a reaction prevention layer (monocrystalline material B) made of a material which has a higher melting point or thermal stability than that of a gallium nitride group **semiconductor** (**semiconductor** crystal A), e.g., SiC and AlN, on a base substrate (Si substrate), a reaction part described above is not formed around silicon interface when the gallium nitride group **semiconductor** (**semiconductor** crystal A) is grown by crystal growth for a long time. By forming a lot of projection parts, the gallium nitride group **semiconductor** (**semiconductor** crystal A) also grows in lateral direction starting from a flat-top portion of the projection part. Then stress between the reaction prevention layer and the **semiconductor** crystal A is remarkably relaxed. Because cracks which penetrate in longitudinal direction are hardly generated on the reaction prevention layer and the Si substrate can be completely interrupted by the reaction prevention layer, reaction preventing effect becomes more secure.

A **seed layer** comprising a GaN **layer** 103 (second **seed layer**) and an AlN buffer **layer** 102 (first **seed layer**) is formed on a sapphire substrate 101 and then the surface of the **seed layer** is etched in stripe pattern whose width of a stripe (width S of a seed) ≈5 μm, width W of a wing ≈15 μm and depth ≈0.5 μm. Then mesas each of whose sectional form is a rectangular are formed, each erosion remains part having plural numbers of **seed layers** at its flat-top portion is formed at arrangement period L≈20 μm and a portion of the sapphire substrate 101 is exposed at the valley part of each wing. Preferably ratio of width of a seed toward a wing, or S/W, may be about 1/3. Then by growing the **semiconductor** crystal A to have thickness of 50 μm or more and by separating it from base substrate, a single crystal of high quality which is independent from the base substrate is obtained.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:162325 USPATFULL

TI Production method for **semiconductor** crystal and **semiconductor** luminous element

IN Nagai, Seiji, Aichi, JAPAN
Tomita, Kazuyoshi, Aichi, JAPAN
Yamazaki, Shiro, Aichi, JAPAN

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      (FILE 'HOME' ENTERED AT 12:49:01 ON 01 FEB 2005)

      FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2, INPADOC' ENTERED AT
      12:49:25 ON 01 FEB 2005
L1          4704 S (GROUP(W)III)(6A)(NITRIDE#)
L2       2445523 S (SEMICONDUCTOR#)
L3         38838 S (LAMINAT? OR COAT? OR LAYER? OR DEPOSIT?)(8A)(SEED# OR SEED#(
L4         23939 S (SUBSTRATE)(6A)(START? OR BEGIN?)
L5         67436 S (CHEMICAL OR PHYSICAL?)(8A)(ETCH?)
L6         14637 S (SEED(W)LAYER#)
L7          4636 S (HALIDE)(6A)(VAPOR OR VAPOR(W)PHASE)
L8             2 S L1 AND L2 AND L3 AND L4 AND L5 AND L6 AND L7

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